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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/689,680

10/13/2000

Ville Eerola

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EXAMINER

BAYARD, EMMANUEL

ART UNIT

PAPER NUMBER

2631

DATE MAILED: 02/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/689,680

Applicant(s)

EEROLA ET AL.

Examiner

Emmanuel Bayard

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

This is in response to amendment filed on 8/19/04 in which claims 1-19 are pending. The applicant's arguments have been fully considered but they are not persuasive enough. Therefore this case is made final. (See Examiner response to arguments below).

#### ***Claim Objections***

Claim 9 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim 1 and 7. See MPEP § 608.01(n).

Accordingly, the claim 9 refers to two claims in conjunction and is not been further treated on the merits.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 3718 of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this

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application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 9-19 are rejected under 35 U.S.C. 102(e) as being anticipated Nagatani et al U.S. Patent No 6,496,474 B1.

As per claim 1, Nagatani et al discloses a device for generating a t least one code phase, comprising: a shift register comprising N outputs (see figs.2, 6, - 15, 18 elements 3, 41, 72 and col.4, lines 5-17) and input to which a data generator is the same as the claimed (code sequence) (see element 1 and col.4, lines 4-17) to be phased is applied, N being an integer greater than two; a M sequence generator is considered as the claimed (at least one logic branch) (see figs. 2, 6-15, 16 elements 3, 42, 51, 61 and col.4, lines 7-67 and col.5, lines 1-5 and col.6, lines 33-50), controlled by at least a clock generator is the same as the claimed (one combination control signal) (see fig.2 element 4 and col.4, lines 11-14), on the basis of which the logic branch adds is considered as the claimed (combines) (see figs. 2, 3a elements 12-13 and col.4, lines 37-50 and col.5, lines 1-18) the code phase from I outputs of the shift register, I being an integer between 2 and N.

As per claim 2, the device of Nagatani does include (I two-input selectors) (see fig.7, 11-13 elements SW52 and col.7, lines 10-35), to the first input of each of which is connected one input of the shift register and to the second input is connected one combination control signal and adders is considered as the claimed (I-input combiner) (see fig.7), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained.

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As per claim 3, the device of Nagatani does include a first logic branch comprising M1 two-input selectors (see fig.7, 11-13) to which the outputs of M1 registers of the shift register and M1 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and M1-input combiner (see fig.7, 11-13), to whose inputs are connected the outputs of said M1 selectors and from whose output the first code phase is obtained (see fig.7, 11-13) ; a second logic branch comprising M2 two-input selectors ((see fig.7, 11-13) to which the outputs of M2 registers of the shift register and M2 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M2-input combiner (see fig.7, 11-13) to whose inputs are connected the outputs of said M2 selectors and from whose output the second code phase is obtained (((see fig.7, 11-13).

As per claim 9, the device of Nagatani inherently includes a software.

As per claim 10, the device of Nagatani inherently includes multipliers and/or AND gates.

As per claim 11, the device of Nagatani does include are adders and/or OR gates (see fig.3a).

As per claim 12, the device of Nagatani inherently includes tap is considered as the claimed weighting coefficients.

As per claims 13 and 16, the device of Nagatani discloses a correlator comprising: generation means comprising a code generator for generating local

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code (see fig.2 element 10 and col.5, lines 14-15), and a shift register (see figs.2, 6, -15, 18 elements 3, 41, 72 and col.4, lines 5-17), the generation means generating at least one code phase from said local code; at least matched filter is functionally equivalent to the claimed (to at least one correlator) (see fig.17 element 123 col.5, lines 55-57 and col.11, lines 20-25 and col.13, lines 30-31) for correlating a signal applied to the correlator structure with said at least on locally generated code phase, said generation means further comprising a M sequence generator is considered as the claimed (at least one logic branch) (see figs. 2, 6-15, 16 elements 3, 42, 51, 61 and col.4, lines 7-67 and col.5, lines 1-5 and col.6, lines 33-50), controlled by at least a clock generator is the same as the claimed (one combination control signal) (see fig.2 element 4 and col.4, lines 11-14), on the basis of which the logic branch adds is considered as the claimed (combines) (see fig.3a ) the code phase from I outputs of the shift register, I being an integer between 2 and N.

As per claims 14 and 17, the correlator of Nagatani does include (I two-input selectors) (see fig.7, 11-13 elements SW52 and col.7, lines 10-35), to the first input of each of which is connected one input of the shift register and to the second input is connected to one combination control signal and adders is considered as the claimed (I-input combiner) (see fig.7), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained.

As per claims 15 and 18, the device of Nagatani inherently includes software.

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As per claim 19 the device of Nagatani inherently includes spreading code replica.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatani U.S. Patent No 6,496,474 B1 in view of Nakamura et al U.S. Patent NO 6,275,520 B.

2. As per claims 4-6, Nagatani teaches all the features of the claimed invention except a third logic branch connected directly to the output of one register of the shift register and from which the third code phase is obtained.

Nakamura et al teaches a third branch (see figs.2, 9 element 16) connected directly to the output of one register of the shift registers (see fig.2 element 10) and from which the third code phase is obtained (see col.1, lines 36-45 and col.2, lines 60-65).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Nakamura into Nagatani as to provide desired shift amounts and each pattern would be prestored in the storage location in the ROM as taught by Nakamura (see col.2, lines 63-65).

As per claims 7-8, Nagatani teaches all the features of the claimed invention except a fourth logic branch connected directly to the output of one register of the shift register and from which the third code phase is obtained.

Nakamura et al teaches a fourth branch (see figs.2, 9 element 16) connected directly to the output of one register of the shift registers (see fig.2 element 10) and from which the third code phase is obtained (see col.1, lines 36-45 and col.2, lines 60-65).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Nakamura into Nagatani as to provide desired shift amounts and each pattern would be prestored in the storage location in the ROM as taught by Nakamura (see col.2, lines 63-65).

### ***Response to Arguments***

1. Applicant's arguments filed 8/19/04 have been fully considered but they are not persuasive.

In page 3, paragraph 2 of the response applicant argues that the combination control signals of the independent claims are used "to set weighting coefficients for the output of the shift registers". Examiner respectfully disagrees because none of the independent claim teaches such limitation (control signals to set weighting coefficients) for the output of the shift registers and there is evidence into the claims to support such arguments. Since the claims limitation are broad, examiner is entitled to interpret the claim limitation as it's presented or writing in the application. Therefore the claims stand rejected as stated in the office action dated 4/18/04 and this case is made final.



***Conclusion***

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

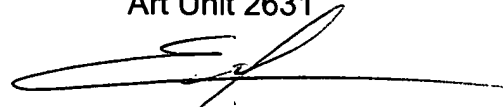
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard  
Primary Examiner  
Art Unit 2631

2/14/05

  
**EMMANUEL BAYARD**  
**PRIMARY EXAMINER**